

## X-BAND MONOLITHIC SERIES FEEDBACK LNA

Randall E. Lehmann and David D. Heston

Texas Instruments Incorporated  
13500 N. Central Expressway  
Dallas, Texas 75266

### ABSTRACT

An X-band monolithic three-stage low noise amplifier (LNA) employing series feedback has demonstrated 1.8 dB noise figure with 30.0 dB gain and an input VSWR less than 1.2:1 at 10 GHz. The key to this design is using monolithic technology to obtain an exactly repeatable series feedback inductance to achieve a simultaneous noise match and input VSWR match.

### INTRODUCTION

In conventional LNAs the common-source FET input stage is presented with an optimum noise match ( $Z_{opt}$ ) to achieve minimum noise figure at the expense of exhibiting high input VSWR. However, to achieve optimum noise figure and low input VSWR simultaneously for a single-ended amplifier, series feedback provides the solution. This is the first reported demonstration of the use of series feedback in a monolithic microwave integrated circuit (MMIC) to achieve state-of-the-art X-band performance.

### HISTORY

Strutt and Van Der Ziel in their 1942 article "Suppression of Spontaneous Fluctuations in Amplifiers and Receivers for Electrical Communication and Measuring Devices," reported that a feedback inductor inserted into the cathode lead of a common-cathode high vacuum triode circuit might enhance the signal-to-noise ratio at high frequencies. (1)

In 1974, Jakob Engberg presented equations as well as optimization procedures for the design of two-port low noise amplifiers. (2) Engberg describes how a combination of shunt and series feedback and proper output loading can be used to achieve  $Z_{opt} = S_{11}^*$ . As only lossless feedback elements are used, Engberg states that the minimum noise measure,  $M_{min}$ , remains constant. He reports that this theory has been verified at UHF frequencies using hybrid circuits. Other researchers (3,4,5) have demonstrated hybrid amplifiers which employ reactive feedback for improved performance.

Monolithic technology provides the key in obtaining an exactly repeatable series feedback inductance. A high impedance microstrip

transmission line can be accurately modeled and reproduced in large quantity. Optimization of bond wire lengths to achieve the correct feedback impedance, as in a hybrid amp, is eliminated.

### DEVICE CHARACTERIZATION

A 0.5  $\mu\text{m}$  gate-width FET, shown in Figure 1, is used in each of the three stages. The device incorporates reactively ion-etched vias through 0.15  $\mu\text{m}$  thick GaAs to provide source grounding. Gate and drain terminals are brought to single bond pads to facilitate implementation into a monolithic circuit. The "monolithic-discrete" device is processed identically to the final MMIC, including deposition of the correct silicon nitride thickness to be used for the metal-insulator-metal (MIM) capacitors. This ensures that any change or increase in gate-drain and gate-source capacitances resulting from the increased capacitor dielectric thickness, which is greater than the standard discrete FET passivation thickness, is accounted for in the device characterization. The discrete FET is also fabricated on the same thickness GaAs as the MMIC so that the inductance of the vias can be properly modeled.

Several slices of these "monolithic-discrete" devices were evaluated for minimum noise figure (NF) and associated gain at 10 GHz. Table I shows a summary of the measured results from the 75 FETs tested. The minimum NF and associated gain are listed for both the best and worst FET measured as well as the numerical average of all 75 FETs.

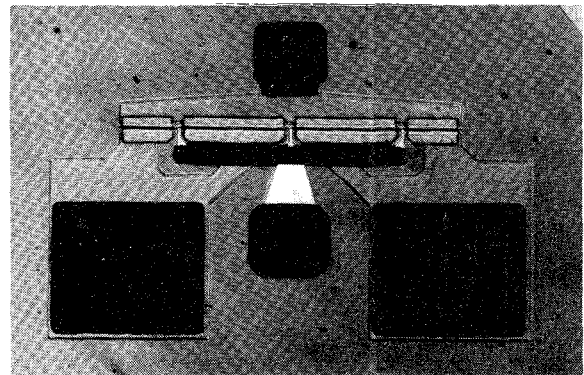


Figure 1. "Monolithic-discrete" FET

Table I: Noise Figure and Gain Data for "Monolithic Discrete" FETs at 10 GHz

TOTAL NUMBER FETs TESTED	NFmin (dB)			Associated Gain (dB)		
	LO	HI	AVG.	LO	HI	AVG.
75	1.5	1.9	1.7	9.5	11.5	11.0

### CIRCUIT DESIGN

Implementation of series feedback provides several advantages for low noise amplifier design. Inductive reactance in the source lead of a common-source FET increases the real part of the input impedance. With proper impedance loading at the output of the FET, the conjugate of the FET input impedance and the optimum noise match impedance become coincident. Figure 2 illustrates the effect of the series feedback on  $S_{11}^*$  and  $Z_{opt}$  at 10 GHz. Series feedback decreases the equivalent noise resistance,  $r_n$ , of the two-port (device plus feedback) as well as decreasing the sensitivity to changes in the intrinsic device properties. Because inductive series feedback increases the real part of the input impedance, the stability of the device is enhanced. Inductive series feedback requires no dc blocking capacitor as in the case of shunt feedback. The feedback inductor (high impedance line) can be realized monolithically in a very repeatable, high yield manner. The monolithic feed-back element is fabricated on the semi-insulating GaAs substrate at the same process step as the rf transmission lines and the bottom plates of the MIM capacitors. No additional process steps or increased complexity are required.

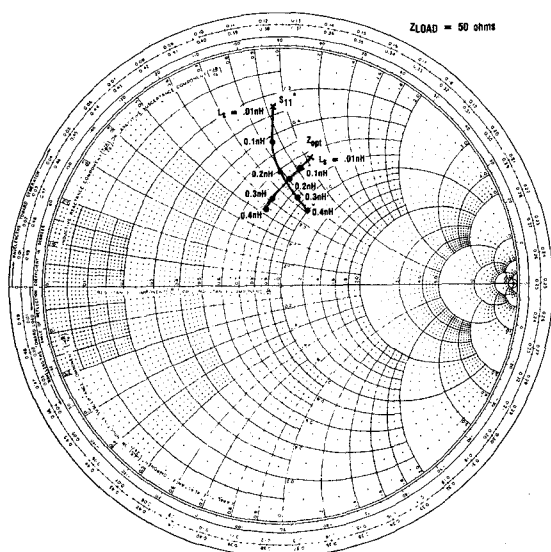


Figure 2. Impedance Mapping of  $S_{11}^*$  and  $Z_{opt}$  at 10 GHz

The three-stage LNA circuit design is shown in Figure 3. All rf matching and dc bias circuitry is included on the monolithic chip, shown in Figure 4. The chip size is  $3.0 \times 2.3 \times 0.15 \mu\text{m}$ . Via holes are etched through the substrate and filled with gold to form low resistance, low inductance ground connections for the sources of the FET and the rf bypass capacitors. The gate and drain bias voltages are brought to common points at opposite corners of the chip. Gold-germanium-nickel-gold resistors are inserted in the gate bias line to improve low frequency stability.

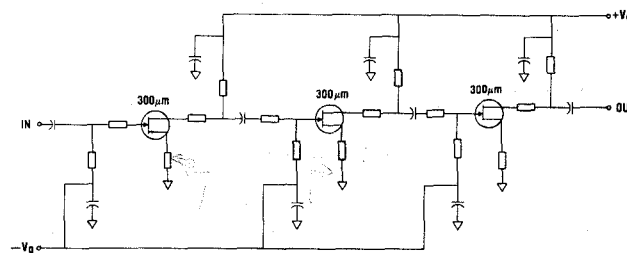


Figure 3. Monolithic Three-stage LNA Circuit Schematic

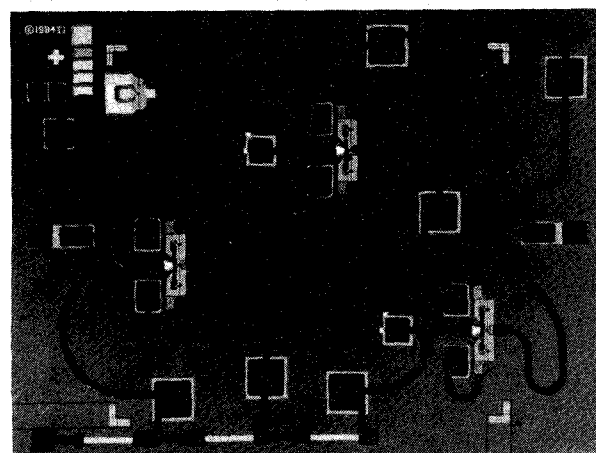


Figure 4. Monolithic Three-stage LNA

### RF PERFORMANCE

The monolithic three-stage LNA with series feedback has demonstrated a 1.8 dB noise figure with 30.0 dB gain and an input VSWR less than 1.2:1 at 10 GHz. The X-band gain and noise figure response is shown in Figure 5. Maximum noise figure is 2.0 dB from 8.5 to 11.5 GHz. From 9.0 to 11 GHz input VSWR is less than 1.8:1. The input and output VSWR response is illustrated in Figure 6. The amplifier is operated at a drain bias of 3 volts and a total drain current of 30 mA. Output power at 1 dB gain compression is 10 dBm.

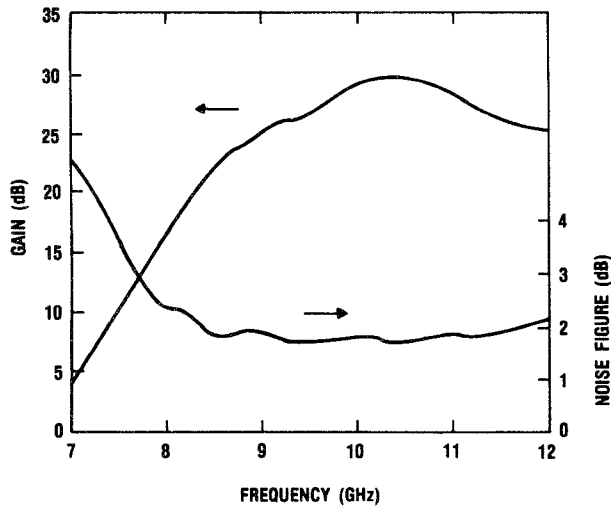


Figure 5. LNA Gain and Noise Figure Performance

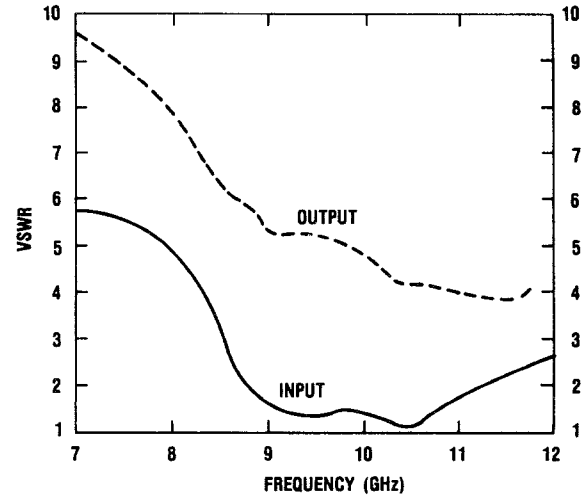


Figure 6. LNA VSWR Performance

Thirty-five LNAs from nine different slices have been evaluated for NF, gain and VSWR. Table II shows a summary of the results obtained from each slice at 10 GHz. LNAs were evaluated at bias conditions for minimum NF. The best and worst LNA measured as well as the average of all LNAs from that slice are recorded.

### CONCLUSIONS

An X-band monolithic three-stage LNA using series feedback has demonstrated excellent gain, noise figure and input VSWR performance. Results from thirty-five LNAs from nine slices highlight the advantages of a series feedback design to achieve very repeatable performance.

Table II: Slice Summary of LNA Measurements at 10 GHz

SLICE #	# LNAs TESTED	NF (dB)			GAIN (dB)			INPUT VSWR		
		LO	HI	AVG.	LO	HI	AVG.	LO	HI	AVG.
1	10	1.9	2.2	2.0	28.2	32.4	30.0	1.1	1.4	1.2
2	4	1.8	2.0	1.9	29.5	32.0	30.9	1.2	1.4	1.3
3	4	1.9	2.0	1.9	28.3	32.1	30.4	1.1	1.4	1.2
4	4	1.9	2.2	2.0	26.5	31.6	28.7	1.1	1.2	1.2
5	2	2.3	2.4	2.3	27.2	27.6	27.4	1.3	1.3	1.3
6	4	2.0	2.1	2.1	28.7	30.8	30.0	1.1	1.3	1.2
7	5	2.1	2.4	2.2	25.1	29.3	26.9	1.1	1.4	1.2
8	1	2.2	2.2	2.2	30.0	30.0	30.0	1.4	1.4	1.4
9	1	2.0	2.0	2.0	30.1	30.1	30.1	1.4	1.4	1.4
TOTAL	35	1.8	2.4	2.0	25.1	32.4	29.4	1.1	1.4	1.2

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